

SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

SDLS006

D2634, JANUARY 1981 (REVISED MARCH 1988)

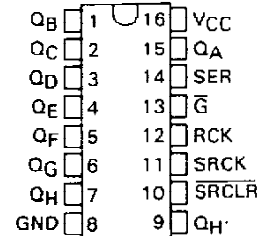
- 8-Bit Serial-In, Parallel-Out Shift Registers with Storage
- Choice of 3-State ('LS595) or Open-Collector ('LS596) Parallel Outputs
- Shift Register Has Direct Clear
- Accurate Shift Frequency: DC to 20 MHz

description

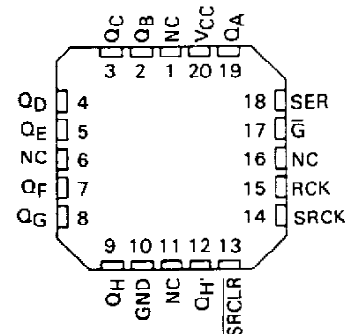
These devices each contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. The storage register has parallel 3-state ('LS595) or open-collector ('LS596) outputs. Separate clocks are provided for both the shift register and the storage register. The shift register has a direct-overriding clear, serial input, and serial output pins for cascading.

Both the shift register and storage register clocks are positive-edge triggered. If the user wishes to connect both clocks together, the shift register state will always be one clock pulse ahead of the storage register.

SN54LS595, SN54LS596 . . . J OR W PACKAGE
SN74LS595, SN74LS596 . . . N PACKAGE
(TOP VIEW)



SN54LS595, SN54LS596 . . . FK PACKAGE
(TOP VIEW)



NC - No internal connection

schematics of inputs and outputs



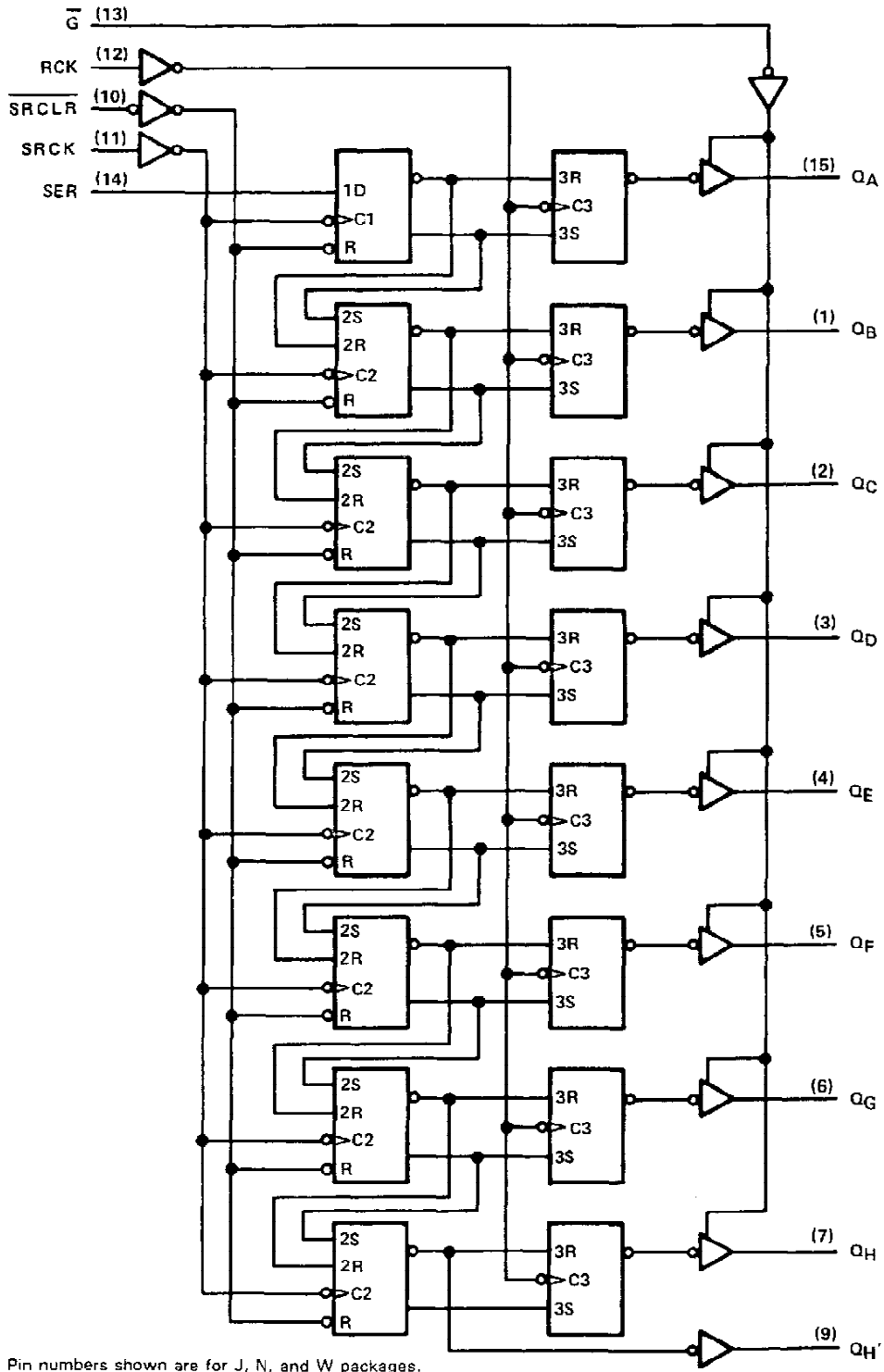
PRODUCTION DATA documents contain information current as of publication date. Products conform to specifications per the terms of Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

TEXAS
INSTRUMENTS

POST OFFICE BOX 656012 • DALLAS, TEXAS 75265

SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

logic diagram (positive logic)



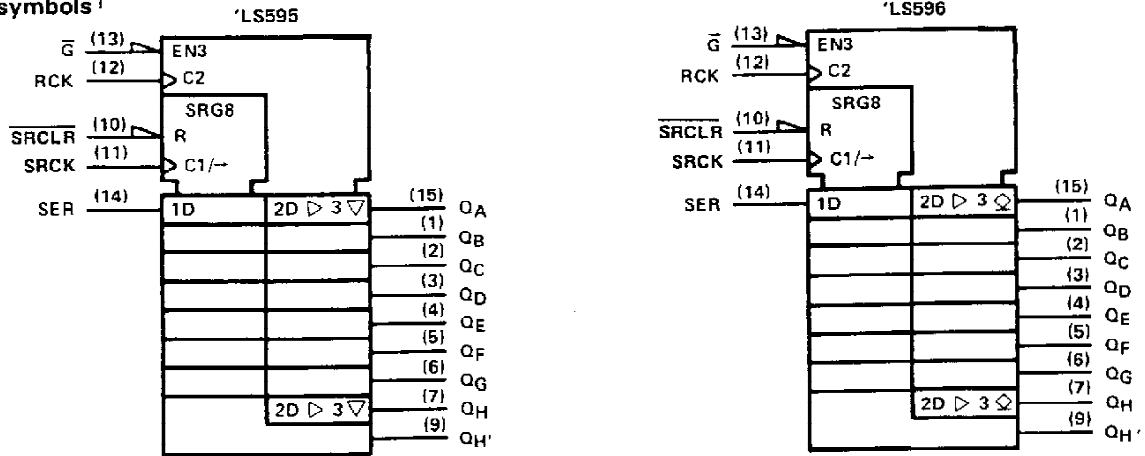
Pin numbers shown are for J, N, and W packages.

TEXAS
INSTRUMENTS

POST OFFICE BOX 655012 • DALLAS, TEXAS 75265

SN54LS595, SN54LS596, SN74LS595, SN74LS596 8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

logic symbols †



†These symbols are in accordance with ANSI/IEEE Std. 91-1984 and IEC Publication 617-12. Pin numbers shown are for J, N, and W packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)	7 V
Input voltage	7 V
Off-state output voltage	5.5 V
Operating free-air temperature range: SN54LS595, SN54LS596	-55°C to 125°C
SN74LS595, SN74LS596	0°C to 70°C
Storage temperature range	-65°C to 150°C

NOTE 1: Voltage values are with respect to the network ground terminal.

recommended operating conditions

		SN54LS'			SN74LS'			UNIT
		MIN	NOM	MAX	MIN	NOM	MAX	
V_{CC}	Supply voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH}	High-level input voltage	2			2			V
V_{IL}	Low-level input voltage	0.7			0.8			V
V_{OH}	High-level output voltage			5.5			5.5	V
I_{OH}	High-level output current			-1			-1	mA
				-1			-2.6	
I_{OL}	Low-level output current			8			16	mA
				12			24	
f_{SRCK}	Shift clock frequency	0		20	0		20	MHz
$t_w(SRCK)$	Duration of shift clock pulse	25			25			ns
$t_w(RCK)$	Duration of register clock pulse	20			20			ns
$t_w(SRCLR)$	Duration of shift clear pulse, low level	20			20			ns
t_{su}	Setup time	SRCLR inactive before SRCK †		20	20		ns	
		SER before SRCK †		20	20			
		SRCK † before RCK † (see Note 2)		40	40			
		SRCLR low before RCK †		40	40			
t_h	Hold time	0			0		ns	
T_A	Operating free-air temperature	-55		125	0		70	°C

NOTE 2: This setup time ensures the register will see stable data from the shift-register outputs. The clocks may be connected together, in which case the storage register state will be one clock pulse behind the shift register.



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SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS †	SN54LS*		SN74LS*		UNIT		
		MIN	TYP ‡	MAX	MIN		TYP ‡	MAX
V _{IK}	V _{CC} = MIN, I _I = -18 mA			-1.5		-1.5	V	
V _{OH}	'LS595 Q Q _H '	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OH} = -1 mA	2.4	3.2			
			I _{OH} = -2.6 mA			2.4	3.1	
			I _{OH} = -1 mA	2.4	3.2	2.4	3.2	
I _{OH}	'LS596 Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 5.5 V					0.1	mA
V _{OL}	Q	V _{CC} = MIN, V _{IH} = 2 V, V _{IL} = MAX	I _{OL} = 12 mA	0.25	0.4	0.25	0.4	V
			I _{OL} = 24 mA			0.35	0.5	
			I _{OL} = 8 mA	0.25	0.4	0.25	0.4	
			I _{OL} = 16 mA			0.35	0.5	
I _{OZH}	'LS595 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 2.7 V			20		20	μA
I _{OZL}	'LS595 Q	V _{CC} = MAX, V _{IH} = 2 V, V _{IL} = MAX, V _{OH} = 0.4 V			-20		-20	μA
I _I		V _{CC} = MAX, V _I = 7 V			0.1		0.1	mA
I _{IH}		V _{CC} = MAX, V _I = 2.7 V			20		20	μA
I _{IL}	SER	V _{CC} = MAX, V _I = 0.4 V			-0.4		-0.4	mA
	All others				-0.2		-0.2	
I _{OS} §	'LS595 Q	V _{CC} = MAX, V _O = 0 V			-30		-130	mA
	Q _H '				-20		-100	
I _{CCH}	'LS595	V _{CC} = MAX, All possible inputs grounded, All outputs open			33		50	mA
	'LS596				30		45	
I _{CCL}	'LS595	All possible inputs grounded, All outputs open			42		65	mA
	'LS596				36		55	
I _{CCZ}	'LS595			44		65	mA	

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions.

‡ All typical values are at V_{CC} = 5 V, T_A = 25°C.

§ Not more than one output should be shorted at a time, and duration of the short-circuit should not exceed one second.

TEXAS
INSTRUMENTS

POST OFFICE BOX 855012 • DALLAS, TEXAS 75265

SN54LS595, SN54LS596, SN74LS595, SN74LS596
8-BIT SHIFT REGISTERS WITH OUTPUT LATCHES

switching characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$ (see note 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS	'LS595			'LS596			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
t_{PLH}	SRCK ↑	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	12	18		14	21	ns	
t_{PHL}				17	25		20	30	ns	
t_{PLH}	RCK ↑	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$	12	18		28	42	ns	
t_{PHL}				24	35		24	35	ns	
t_{PZH}	\overline{G} ↓	Q_A thru Q_H		20	30				ns	
t_{PZL}				25	38				ns	
t_{PHZ}	\overline{G} ↑	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 5\text{ pF}$	20	30				ns	
t_{PLZ}				25	38				ns	
t_{PLH}	\overline{G} ↑	Q_A thru Q_H	$R_L = 667\ \Omega$, $C_L = 45\text{ pF}$				40	60	ns	
t_{PHL}	\overline{G} ↓	Q_A thru Q_H					25	38	ns	
t_{PHL}	SRCLR ↓	Q_H'	$R_L = 1\text{ k}\Omega$, $C_L = 30\text{ pF}$	24	35		24	35	ns	

NOTE 3: Load circuits and voltage waveforms are shown in Section 1.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-86717012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8671701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8671701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8671701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-8671701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS595N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS595NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS596D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS596D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS596NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS596NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54LS595FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS595FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS595W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS595W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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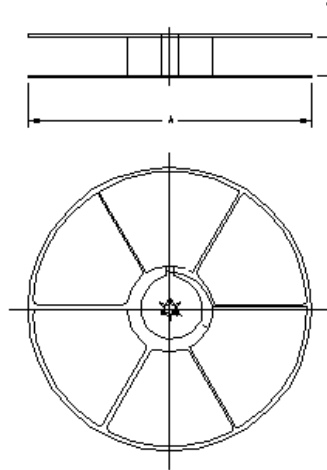
Carrier tape design is defined largely by the component length, width, and thickness.

A_o = Dimension designed to accommodate the component width.
B_o = Dimension designed to accommodate the component length.
K_o = Dimension designed to accommodate the component thickness.
W = Overall width of the carrier tape.
P = Pitch between successive cavity centers.



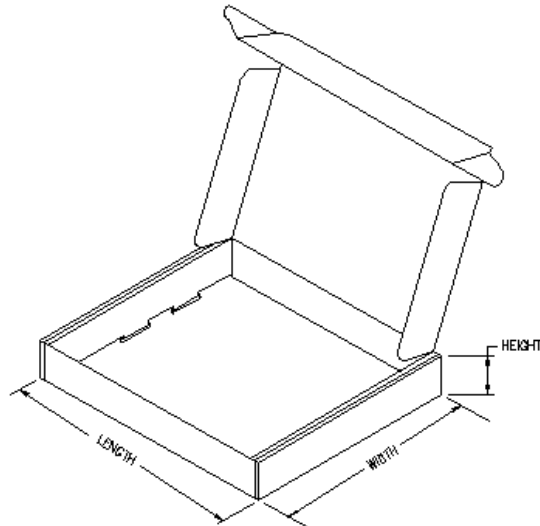
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS595DR	D	16	FMX	330	16	6.5	10.3	2.1	8	16	Q1
SN74LS595NSR	NS	16	MLA	330	16	8.2	10.5	2.5	12	16	Q1



TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LS595DR	D	16	FMX	342.9	336.6	28.58
SN74LS595NSR	NS	16	MLA	342.9	336.6	28.58



J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



4040180-3/D 07/03

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



4040140/D 10/96

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
5962-86717012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
5962-8671701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8671701EA	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
5962-8671701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
5962-8671701FA	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SN54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SN74LS595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS595N3	OBSOLETE	PDIP	N	16		TBD	Call TI	Call TI
SN74LS595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS595NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
						no Sb/Br)		
SN74LS595NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS595NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74LS596D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS596D	OBSOLETE	SOIC	D	16		TBD	Call TI	Call TI
SN74LS596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS596N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS596NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74LS596NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SNJ54LS595FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS595FK	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	N / A for Pkg Type
SNJ54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS595J	ACTIVE	CDIP	J	16	1	TBD	A42 SNPB	N / A for Pkg Type
SNJ54LS595W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type
SNJ54LS595W	ACTIVE	CFP	W	16	1	TBD	A42	N / A for Pkg Type

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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TAPE AND REEL BOX INFORMATION



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LS595DR	D	16	SITE 27	330	16	6.5	10.3	2.1	8	16	Q1
SN74LS595NSR	NS	16	SITE 41	330	16	8.2	10.5	2.5	12	16	Q1

TAPE AND REEL BOX DIMENSIONS



Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
SN74LS595DR	D	16	SITE 27	342.9	336.6	28.58
SN74LS595NSR	NS	16	SITE 41	346.0	346.0	33.0

J (R-GDIP-T**)

14 LEADS SHOWN

CERAMIC DUAL IN-LINE PACKAGE



DIM \ PINS **	14	16	18	20
A	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC	0.300 (7,62) BSC
B MAX	0.785 (19,94)	.840 (21,34)	0.960 (24,38)	1.060 (26,92)
B MIN	—	—	—	—
C MAX	0.300 (7,62)	0.300 (7,62)	0.310 (7,87)	0.300 (7,62)
C MIN	0.245 (6,22)	0.245 (6,22)	0.220 (5,59)	0.245 (6,22)



4040083/F 03/03

- NOTES:
- All linear dimensions are in inches (millimeters).
 - This drawing is subject to change without notice.
 - This package is hermetically sealed with a ceramic lid using glass frit.
 - Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
 - Falls within MIL STD 1835 GDIP1-T14, GDIP1-T16, GDIP1-T18 and GDIP1-T20.

W (R-GDFP-F16)

CERAMIC DUAL FLATPACK



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a ceramic lid using glass frit.
 - D. Index point is provided on cap for terminal identification only.
 - E. Falls within MIL STD 1835 GDFP1-F16 and JEDEC MO-092AC

FK (S-CQCC-N**)

LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. This package can be hermetically sealed with a metal lid.
 - D. The terminals are gold plated.
 - E. Falls within JEDEC MS-004

N (R-PDIP-T**)

PLASTIC DUAL-IN-LINE PACKAGE

16 PINS SHOWN



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



4040047-4/H 11/2006

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

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